Question solve 2020 – 21 :

1 ) Define opcode . describe the fetch execute cycle of a microprocessor with an example.   
**Solution :** Here’s a **short 3-marks style answer** 👇

**Opcode**

The **Opcode (Operation Code)** is the part of an instruction set in a microprocessor that specifies the **operation to be performed** (e.g., ADD, SUB, MOV).

**Fetch–Execute Cycle**

The **fetch–execute cycle** is the process by which a microprocessor runs instructions:

1. **Fetch** – The CPU fetches the instruction (opcode) from memory using the Program Counter (PC).
2. **Decode** – The instruction is decoded to understand what operation is required.
3. **Execute** – The CPU performs the operation (e.g., add numbers, move data).

**Example**

Instruction: ADD A, B

* **Fetch**: Opcode for ADD is fetched. R1, R2 হলো **operands**।
* **Decode**: CPU understands it must add contents of register B to A.
* **Execute**: Result is stored in register A.

### Q2. Suppose, AX contains 5ABCh and BX contains 21FCh. Find the difference of AX and BX by using complementation and addition operation.

We need to calculate:

#### **Step 1: Write the values in hexadecimal**

* AX = **5ABC**h
* BX = **21FC**h

#### **Step 2: Concept of subtraction using 2’s complement**

In microprocessor, subtraction is usually done like this:

AX−BX=AX+(2’s complement of BX)AX - BX = AX + (2’s\ complement\ of\ BX)

So, first we calculate 2’s complement of BX.

#### **Step 3: 1’s complement of BX**

BX = **21FC**h  
1’s complement = FFFFh – 21FCh

FFFFh−21FCh=DE03hFFFF\_h - 21FC\_h = DE03\_h

#### **Step 4: 2’s complement of BX**

Add 1 to the 1’s complement:

DE03h+1h=DE04hDE03\_h + 1\_h = DE04\_h

So, **2’s complement of BX = DE04h**.

#### **Step 5: Perform addition**

Now,

AX−BX=AX+(2’s complement ofBX)AX - BX = AX + (2’s\ complement\ of BX) =5ABCh+DE04h= 5ABC\_h + DE04\_h

Add them:

5ABC

+ DE04

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38C0 (with carry)

* Total = **13,960h**
* Since we are working with 16-bit registers, only the lower 16-bit result is kept.
* Lower 16-bit = **38C0h**
* Carry is discarded.

#### ✅ Final Answer:

AX−BX=38C0hAX - BX = 38C0\_h

👉 **So, the difference of AX (5ABCh) and BX (21FCh) using complementation and addition operation is 38C0h.**

### ****Q3. What are data registers? Write down the special features of 80286 μP over 8086 μP.****

#### **(a) Data Registers**

* Data registers হলো microprocessor এর ভিতরের high-speed storage location।
* এগুলো মূলত **temporary data, intermediate result, arithmetic ও logical operation** এর জন্য ব্যবহার হয়।
* 8086/80286 এ ৪টা প্রধান data register থাকে, যেগুলো general purpose ও হিসাবে কাজ করে:

1. **AX (Accumulator Register):** Arithmetic, logic, I/O operations এ ব্যবহৃত হয়।
2. **BX (Base Register):** Addressing এ কাজে লাগে।
3. **CX (Count Register):** Looping ও shifting এর জন্য ব্যবহৃত হয়।
4. **DX (Data Register):** Multiplication, Division, এবং I/O operations এ ব্যবহার হয়।

👉 প্রতিটা 16-bit data register আবার 2 ভাগে ভাগ করা যায় (High ও Low 8-bit):

* AX → AH, AL
* BX → BH, BL
* CX → CH, CL
* DX → DH, DL

#### **(b) Special Features of 80286 μP over 8086 μP**

| **Feature** | **8086** | **80286,80186** |
| --- | --- | --- |
| **Data Bus** | 16-bit | 16-bit |
| **Address Bus** | 20-bit (1 MB memory access) | 24-bit (16 MB memory access) |
| **Operating Modes** | Real Mode only | Real Mode + Protected Mode |
| **Memory Management** | No protection, only segmentation | Advanced segmentation + Protection |
| **Performance** | 5–10 MHz | 8–12.5 MHz (faster) |
| **Multitasking** | Not supported | Supported with memory protection |
| **Virtual Memory** | Not available | Available (up to 1 GB virtual memory) |

✅ **Summary (Exam-Ready):**

* **Data registers** হলো temporary storage registers (AX, BX, CX, DX), যেগুলো arithmetic, logical ও addressing operation এ ব্যবহৃত হয়।
* **80286 μP** এর প্রধান সুবিধা 8086 এর উপর হলো: বড় memory access (16 MB), protected mode, multitasking support, এবং virtual memory support।

**Q4.** What is memory segment? Translate the following high-level code into equivalent assembly code.  
  A = B – 2 × A (03)

**What is Memory Segment?**

A **memory segment** is a block (portion) of memory in the microprocessor’s address space that is used for a specific purpose, such as:

* **Code Segment (CS):** stores program instructions.
* **Data Segment (DS):** stores variables/data.
* **Stack Segment (SS):** stores stack information (function calls, return addresses).
* **Extra Segment (ES):** used for additional data storage.

In 8086, segmentation allows addressing up to **1 MB of memory** using 16-bit registers with segment:offset addressing.

A screenshot of a computer program

AI-generated content may be incorrect.

**High-Level Code:**

A = B – 2 × A

**Equivalent Assembly Code (Example in 8086 Assembly):**

; Assume A and B are variables in data segment

A screenshot of a computer

AI-generated content may be incorrect.

**Q5.** What is flag register? How does flag affect on MOV operation? Show, how the instruction  
  ADD AL, BL affects flags where AL contains 80h, BL contains 80h. (03)

**Flag Register**

The **flag register** in a microprocessor is a special register that stores the **status of the processor** after an operation.  
It contains individual **flags** such as:

* **Zero Flag (ZF)** → Set if result = 0
* **Sign Flag (SF)** → Set if result is negative (MSB = 1)
* **Carry Flag (CF)** → Set if there is carry/borrow
* **Overflow Flag (OF)** → Set if signed overflow occurs

**Effect of Flag on MOV Operation**

👉 **MOV simply copies data** from source to destination.

* It does **not perform any arithmetic/logic**, so it **does not change any flag**.

**Example Instruction:**

ADD AL, BL

; AL = 80h, BL = 80h

**Step 1 – Operation:**

AL = 80h + 80h = 100h

**Step 2 – Result in 8-bit register:**

* AL = 00h (lower 8 bits stored)
* Carry generated → CF = 1

**Step 3 – Affected Flags:**

* **CF = 1** (carry occurred)
* **ZF = 1** (result = 00h → zero)
* **SF = 0** (result not negative, MSB=0)
* **OF = 1** (signed overflow: +128 + +128 = -0)

✅ **Final Result:**

* AL = 00h
* CF = 1, ZF = 1, OF = 1, SF = 0

**Question solve : 19 – 20**

**Write down the steps to execute a machine instruction. Illustrate the Intel 8086 Microprocessors organization.**

## **Steps to Execute a Machine Instruction**

1. **Fetch** – The instruction is fetched from memory using the Program Counter (PC) and placed in the Instruction Queue.
2. **Decode** – The Control Unit decodes the opcode to identify the operation and operands.
3. **Fetch Operands** – If operands are in memory/register, they are fetched.
4. **Execute** – The Arithmetic Logic Unit (ALU) or other unit performs the operation.
5. **Store Result** – The result is stored in the destination register/memory.
6. **Update PC** – The Program Counter updates to the next instruction.

## **Intel 8086 Microprocessor Organization**

The 8086 has two main units:

1. **Bus Interface Unit (BIU):**
   * Handles instruction fetching, queuing, and memory/IO addressing.
   * Contains **Segment Registers, Instruction Pointer, Instruction Queue**.
2. **Execution Unit (EU):**
   * Decodes and executes instructions.
   * Contains **ALU, General Purpose Registers, Flag Register, Control Circuitry**.

A diagram of a block diagram

AI-generated content may be incorrect.

## **Memory Segment (Definition)**

A **memory segment** is a block (portion) of memory in the microprocessor’s address space used for storing a specific type of information. In Intel processors like 8086/80286, memory is divided into **segments** such as:

* **Code Segment (CS):** program instructions
* **Data Segment (DS):** variables/data
* **Stack Segment (SS):** stack (function calls, return addresses)
* **Extra Segment (ES):** additional data

## **Features of 80286 Microprocessor**

1. **Bit Size:** 16-bit processor.
2. **Clock Speed:** Operates at 6–8 MHz .
3. **Address Bus:** 24-bit → can address up to **16 MB of physical memory**.
4. **Modes of Operation:**
   * **Real Mode** (1 MB memory access, like 8086)
   * **Protected Mode** (full 16 MB access, with memory protection).
5. **Instruction Queue:** 6-byte prefetch queue for pipelining.
6. **Improved Performance:** Faster execution compared to 8086.
7. **Enhanced Protection:** Provides multitasking and memory protection features.

### ****Q: Write down the difference between physical and logical memory. A memory location has physical address 80FD2h. In what segment does it have offset BFD2h?**** (3 Marks)

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**Q: Which Intel microprocessor addresses 1T of memory? What is the purpose of the microprocessor in a microprocessor-based computer? (2 Marks)**

**(a) Intel microprocessor that addresses 1T memory:**  
👉 **Pentium 4 (64-bit mode)** — এটি 40-bit address bus ব্যবহার করে **1 Terabyte (1T)** memory address করতে পারে।

**(b) Purpose of microprocessor:**  
👉 Microprocessor হলো একটি **CPU-on-a-chip**, যা data **fetch, decode, execute** করে। এটি arithmetic, logic, data transfer এবং control operations সম্পাদন করে, ফলে পুরো computer system এর **brain** হিসেবে কাজ করে।

**Question 05 :** Determine the memory location addressed by the following real mode 80286 register combinations: DS = 1000H and DI = 2000H. Also draw the diagram of memory access.

**Definition: Real Mode Addressing**

**Real Mode Addressing** is the memory addressing scheme used by the Intel 8086/8088 microprocessor, where the CPU generates a **20-bit physical memory address** from a **16-bit segment value** and a **16-bit offset value**.

**Step 1: Formula (Real Mode Addressing)**

Physical Address = (Segment × 10h) + Offset

Here,

* **DS = 1000h**
* **DI = 2000h (offset)**

**Step 2: Calculation**

Segment × 10h = 1000h × 10h = 10000h

Physical Address = 10000h + 2000h = 12000h

**Final Physical Address = 12000h**

**Step 3: Diagram of Memory Access**

